Inductive Bias and Depth Efficiency of Convolutional Networks

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Mathematics of Deep Learning, CVPR 2016

Joint work with Nadav Cohen and Or Sharir
Deep SimNets
  N. Cohen, O. Sharir and A. Shashua
  *Computer Vision and Pattern Recognition (CVPR)* 2016

On the Expressive Power of Deep Learning: A Tensor Analysis
  N. Cohen, O. Sharir and A. Shashua
  *Conference on Learning Theory (COLT)* 2016

Convolutional Rectifier Networks as Generalized Tensor Decompositions
  N. Cohen and A. Shashua
  *International Conference on Machine Learning (ICML)* 2016

Inductive Bias of Deep Convolutional Networks through Pooling Geometry
  N. Cohen and A. Shashua
  *arXiv preprint, May 2016*
Expressiveness

The driving force behind deep networks is their expressiveness

Fundamental theoretical questions:

- What kind of functions can different network architectures represent?
- What is the representational benefit of depth?
- Why do functions realized by convolutional networks suit images?
Universality:
Network is able to realize any function if its size (width) is unlimited.
Expressiveness: Basic Concepts

**Universality:**
Network is able to realize any function if its size (width) is unlimited

**Depth efficiency:**
Function realized by deep network of polynomial size requires super-polynomial size for being realized (or approximated) by shallow network.
Expressiveness: Basic Concepts

Universality:
Network is able to realize any function if its size (width) is unlimited

Depth efficiency:
Function realized by deep network of polynomial size requires super-polynomial size for being realized (or approximated) by shallow network

Complete depth efficiency:
The set of functions realizable by deep network for which depth efficiency does not hold is negligible (has measure zero)
Prior works on the expressiveness of deep networks:

- Study universality and only existence of depth efficiency
- Consider only fully-connected networks, not the architectures commonly used in practice (e.g. convolutional networks)
Outline

1. Convolutional Arithmetic Circuits  \textit{(Cohen, Sharir & Shashua, COLT’16)}

2. Convolutional Rectifier Networks  \textit{(Cohen & Shashua, ICML’16)}

3. Expressiveness Beyond Depth Efficiency  \textit{(Cohen & Shashua, arXiv)}
Convolutional Arithmetic Circuits

Convolutional networks:

- locality
- weight sharing (optional)
- linear activation, product pooling

Computation in log-space leads to **SimNets** – new deep learning architecture showing promising empirical performance

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1 *Deep SimNets, Cohen-Sharir-Shashua, CVPR’16*
Convolutional Arithmetic Circuits (C.S.S. COLT’16)

Coefficient Tensor

Function realized by output $y$:

$$h_y(x_1, \ldots, x_N) = \sum_{d_1 \ldots d_N=1}^M A^y_{d_1, \ldots, d_N} \prod_{i=1}^N f_{\theta_{d_i}}(x_i)$$

- $x_1 \ldots x_N$ – input patches
- $f_{\theta_1} \ldots f_{\theta_M}$ – representation layer functions
- $A^y$ – coefficient tensor ($M^N$ entries, polynomials in weights $a^{l,j,\gamma}$)
Shallow Convolutional Arithmetic Circuit

\[ \text{Shallow network (single hidden layer, global pooling):} \]

\[ \text{input } X \rightarrow \text{representation} \rightarrow 1 \times 1 \text{ conv} \rightarrow \text{global pooling} \rightarrow \text{dense (output)} \]

Coefficient tensor \( A^y \) given by classic **CP decomposition**:

\[ A^y = \sum_{\gamma=1}^{r_0} a^{1,1,y}_\gamma \cdot a^{0,1,\gamma} \otimes a^{0,2,\gamma} \otimes \ldots \otimes a^{0,N,\gamma} \]

\( \text{rank}(A^y) \leq r_0 \)
Deep Convolutional Arithmetic Circuit
←→ Hierarchical Tucker Decomposition

Deep network \((L = \log_2 N\) hidden layers, size-2 pooling windows):

\[
\begin{array}{c}
\text{input } X \\
\text{representation} \\
\text{hidden layer } 0 \\
\text{hidden layer } L-1 \quad (L=\log_2 N) \\
\text{dense (output)}
\end{array}
\]

Coefficient tensor \(A^y\) given by **Hierarchical Tucker decomposition**:

\[
\begin{align*}
\phi^{1,j,y} &= \sum_{\alpha=1}^{r_0} a^{1,j,y}_{\alpha} \cdot a^{0,2,j-1,\alpha} \otimes a^{0,2,j,\alpha} \\
&\vdots \\
\phi^{l,j,y} &= \sum_{\alpha=1}^{r_{L-1}} a^{l,j,y}_{\alpha} \cdot \phi^{l-1,2,j-1,\alpha} \otimes \phi^{l-1,2,j,\alpha} \\
&\vdots \\
A^y &= \sum_{\alpha=1}^{r_{L-1}} a^{L,1,y}_{\alpha} \cdot \phi^{L-1,1,\alpha} \otimes \phi^{L-1,2,\alpha}
\end{align*}
\]
Universality

**Fact:**
CP decomposition can realize any tensor $A^y$ given $M^N$ terms

**Implies:**
Shallow network can realize any function given $M^N$ hidden channels

**Fact:**
Hierarchical Tucker decomposition is a superset of CP decomposition if each level has matching number of terms

**Implies:**
Deep network can realize any function given $M^N$ channels in each of its hidden layers

**Convolutional arithmetic circuits are universal**
The rank of tensor $A^y$ given by Hierarchical Tucker decomposition is at least $\min\{r_0, M\}^{N/2}$ almost everywhere w.r.t. decomposition parameters.
Theorem

The rank of tensor $A^y$ given by Hierarchical Tucker decomposition is at least $\min\{ r_0, M \}^{N/2}$ almost everywhere w.r.t. decomposition parameters.

Since rank of $A^y$ generated by CP decomposition is no more than the number of terms (# of hidden channels in shallow network):

Corollary

Almost all functions realizable by deep network cannot be approximated by shallow network with less than $\min\{ r_0, M \}^{N/2}$ hidden channels.
Theorem

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Corollary

Almost all functions realizable by deep network cannot be approximated by shallow network with less than $\min\{r_0, M\}^{N/2}$ hidden channels.

Convolutional arithmetic circuits are completely depth efficient!
Depth Efficiency Theorem – Proof Sketch

- $[A]$ – arrangement of tensor $A$ as matrix (matricization)

- Relation between tensor and Kronecker products: $[A \otimes B] = [A] \circ [B]$

- $\circ$ – Kronecker product for matrices. Holds: $\text{rank}(A \otimes B) = \text{rank}(A) \cdot \text{rank}(B)$

- Implies: $A = \sum_{z=1}^{Z} \lambda_z v_1^{(z)} \otimes \cdots \otimes v_{2^L}^{(z)} \implies \text{rank}[A] \leq Z$

- By induction over $l = 1 \ldots L$, almost everywhere w.r.t. $\{a^{l, j, \gamma}\}_{l, j, \gamma}$:

  $\forall j \in [N/2^l], \gamma \in [r_l]: \text{rank}[\phi^{l, j, \gamma}] \geq (\min\{r_0, M\})^{2^l/2}$

  - Base: “SVD has maximal rank almost everywhere”

  - Step: $\text{rank}[A \otimes B] = \text{rank}([A] \circ [B]) = \text{rank}[A] \cdot \text{rank}[B]$, and “linear combination preserves rank almost everywhere”
A Note about Measure Zero

- Depth Efficiency occurs with probability 1, i.e., besides a set of measure zero, all functions that can be implemented by a deep network of polynomial size, require exponential size in order to be realized (or even approximated) by a shallow network.
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- The set is a zero set of a certain polynomial (based on determinants).

- The zero set of a polynomial is closed, i.e., cannot approximate anything that is not included in the set.

- In other words, the closure of the set is also of measure zero.
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- For example, the set of Rational numbers is of measure zero, but the closure of the set is not of measure zero. It actually fills the entire space.
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- For example, the set of Rational numbers is of measure zero, but the closure of the set is not of measure zero. It actually fills the entire space.

- Therefore, the set of functions that do not satisfy depth efficiency should be viewed as a low-dimensional manifold rather than a scattered set in space.
Outline

1. Convolutional Arithmetic Circuits  
   (Cohen, Sharir & Shashua, COLT'16)

2. Convolutional Rectifier Networks  
   (Cohen & Shashua, ICML'16)

3. Expressiveness Beyond Depth Efficiency  
   (Cohen & Shashua, arXiv)
From Convolutional Arithmetic Circuits to General Convolutional Networks

Transform convolutional arithmetic circuits into general convolutional networks:

- linear activation $\rightarrow$ general point-wise activation $\sigma(\cdot)$
- product pooling $\rightarrow$ general pooling operator $P\{\cdot\}$
Generalized Tensor Decompositions

Convolutional arithmetic circuits correspond to tensor decompositions based on tensor product $\otimes$:

$$(A \otimes B)_{d_1,\ldots,d_{P+Q}} = A_{d_1,\ldots,d_P} \cdot B_{d_{P+1},\ldots,d_{P+Q}}$$
Convolutional arithmetic circuits correspond to tensor decompositions based on tensor product $\otimes$:

$$(\mathcal{A} \otimes \mathcal{B})_{d_1,\ldots,d_{P+Q}} = \mathcal{A}_{d_1,\ldots,d_P} \cdot \mathcal{B}_{d_{P+1},\ldots,d_{P+Q}}$$

For an associative and commutative operator $g : \mathbb{R} \times \mathbb{R} \to \mathbb{R}$, the generalized tensor product $\otimes_g$ is defined by:

$$(\mathcal{A} \otimes_g \mathcal{B})_{d_1,\ldots,d_{P+Q}} = g(\mathcal{A}_{d_1,\ldots,d_P}, \mathcal{B}_{d_{P+1},\ldots,d_{P+Q}})$$

(same as $\otimes$ but with $g$ instead of product)
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(same as $\otimes$ but with $g$ instead of product)

Generalized tensor decompositions are obtained by replacing $\otimes$ with $\otimes_g$.
General Convolutional Networks \[\iff\] Generalized Tensor Decompositions

Define the **activation-pooling operator**:

\[\rho_{\sigma/P}(a, b) := P\{\sigma(a), \sigma(b)\}\]
General Convolutional Networks \iff Generalized Tensor Decompositions

Define the activation-pooling operator:

$$\rho_{\sigma/P}(a, b) := P\{\sigma(a), \sigma(b)\}$$

If $\rho_{\sigma/P}$ is associative and commutative:

Shallow ConvNet with activation $\sigma(\cdot)$ and pooling $P\{\cdot\}$ \iff Generalized CP decomposition with $\otimes_{\rho_{\sigma/P}}$

Deep ConvNet with activation $\sigma(\cdot)$ and pooling $P\{\cdot\}$ \iff Generalized Hierarchical Tucker decomposition with $\otimes_{\rho_{\sigma/P}}$
Convolutional Rectifier Networks

Convolutional networks with:

- **ReLU activation**: \( \sigma(z) = [z]_+ := \max\{z, 0\} \)
- **max/average pooling**: \( P\{c_j\} = \max\{c_j\}/\text{mean}\{c_j\} \)

Most successful deep learning architecture to date

\(^1\text{Sum and average pooling are equivalent in terms of expressiveness}\)
Convolutional Rectifier Networks

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Most successful deep learning architecture to date

Corresponding activation-pooling operators associative and commutative:

- \( \rho_{\text{ReLU}/\text{max}}(a, b) \coloneqq \max\{[a]_+, [b]_+\} = \max\{a, b, 0\} \)
- \( \rho_{\text{ReLU}/\text{sum}}(a, b) \coloneqq [a]_+ + [b]_+ \)

Equivalence with generalized tensor decompositions thus holds!

---

\(^1\) Sum and average pooling are equivalent in terms of expressiveness
Convolutional Rectifier Networks (C.S. ICML’16)

Universality

Claim

Convolutional rectifier networks are universal with max pooling, but not with average pooling

Proof idea

- Generalized CP and Hierarchical Tucker decompositions with $\circledast \rho_{ReLU/max}$ can realize any tensor given sufficient number of terms

- With $\circledast \rho_{ReLU/sum}$ the decompositions generate tensors that have low rank when arranged as matrices
Claim

Convolutional rectifier networks realize depth efficient functions

Proof idea

With $\otimes \rho_{ReLU/\max}$ the rank of a generated tensor arranged as a matrix is:

- **Generalized CP decomposition:**
  Linear in number of terms (# of hidden channels in shallow network)

- **Generalized Hierarchical Tucker decomposition:**
  Exponentially high for appropriately chosen weight settings
Claim

Convolutional rectifier networks are not completely depth efficient

Proof idea

With $\otimes \rho_{\text{ReLU}/\text{max}}$ there exist weight settings $a^{l,j,\gamma}$ for generalized Hierarchical Tucker decomposition such that:

- Realized tensor can be implemented by generalized CP decomposition with single term (single hidden channel in shallow network)
- The same holds if $a^{l,j,\gamma}$ are subject to small perturbations
## Convolutional Rectifier Networks vs. Convolutional Arithmetic Circuits

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¹ *Deep SimNets, Cohen-Sharir-Shashua, CVPR’16*
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\(^1\) *Deep SimNets, Cohen-Sharir-Shashua, CVPR’16*

*Developing optimization methods for convolutional arithmetic circuits may give rise to an architecture that is provably superior but has so far been overlooked.*
Outline

1. Convolutional Arithmetic Circuits  \((Cohen, Sharir & Shashua, COLT'16)\)

2. Convolutional Rectifier Networks  \((Cohen & Shashua, ICML'16)\)

3. Expressiveness Beyond Depth Efficiency  \((Cohen & Shashua, arXiv)\)
Limitations of Depth Efficiency

Depth efficiency implies that there are functions efficiently realizable by deep networks but not by shallow ones.

It does not explain why these functions are effective.

Moreover, it does not compare different networks of the same depth, and thus does not shed light on the **inductive bias** of deep architectures.
The separation rank of a function $h(x_1, \ldots, x_N)$ w.r.t. the partition $I \cup J = [N]$, $I = \{i_1, \ldots, i_{|I|}\}$, $J = \{j_1, \ldots, j_{|J|}\}$:

$$sep(h; I, J) := \min\{R \in \mathbb{N}: \exists g_1 \ldots g_R: \ (R s_{|I|}) \rightarrow R_s \ \cdot \ h(x_1, \ldots, x_N) = \sum_{R \nu = 1}^{R} g_{\nu}(x_{i_1, \ldots, i_{|I|}}) g'_{\nu}(x_{j_1, \ldots, j_{|J|}}) \}$$

Measures correlation induced by $h$ between $(x_{i_1, \ldots, i_{|I|}})$ and $(x_{j_1, \ldots, j_{|J|}})$.

We analyze the separation ranks of convolutional arithmetic circuits.

---

**Partition A**

**Partition B**

$I - \quad \quad J -$
The separation rank of a function $h(x_1, \ldots, x_N)$ w.r.t. the partition $I \cup J = [N], I = \{i_1, \ldots, i_{|I|}\}, J = \{j_1, \ldots, j_{|J|}\}$:

$$sep(h; I, J) := \min \left\{ R \in \mathbb{N} : \exists g_1 \ldots g_R : (\mathbb{R}^s)^{|I|} \to \mathbb{R}, g'_1 \ldots g'_R : (\mathbb{R}^s)^{|J|} \to \mathbb{R} \quad \text{s.t.} \quad h(x_1, \ldots, x_N) = \sum_{\nu=1}^{R} g_{\nu}(x_{i_1}, \ldots, x_{i_{|I|}})g'_{\nu}(x_{j_1}, \ldots, x_{j_{|J|}}) \right\}$$

Measures correlation induced by $h$ between $(x_{i_1} \ldots x_{i_{|I|}})$ and $(x_{j_1} \ldots x_{j_{|J|}})$.

We analyze the separation ranks of convolutional arithmetic circuits.
Recall expression for function realized by convolutional arithmetic circuit:

\[ h_y(x_1, \ldots, x_N) = \sum_{d_1 \ldots d_N=1}^{M} A^y_{d_1,\ldots,d_N} \prod_{i=1}^{N} f_{\theta_{d_i}}(x_i) \]

- \( x_1 \ldots x_N \in \mathbb{R}^s \) – local image patches
- \( A^y \in \mathbb{R}^{M \times \cdots \times M} \) – coefficient tensor, \( N \) modes (indexing entries)
Separation Ranks of Convolutional Arithmetic Circuits

Recall expression for function realized by convolutional arithmetic circuit:

\[
h_y (x_1, \ldots, x_N) = \sum_{d_1 \ldots d_N=1}^{M} A^y_{d_1, \ldots, d_N} \prod_{i=1}^{N} f_{\theta_{d_i}} (x_i)
\]

- \(x_1 \ldots x_N \in \mathbb{R}^s\) – local image patches
- \(A^y \in \mathbb{R}^{M \times \cdots \times M}\) – coefficient tensor, \(N\) modes (indexing entries)

Define \( [A^y]_{I,J} \) – matricization of \( A^y \) w.r.t. the partition \( I \cup J = [N] \):

- Arrangement of \( A^y \) as matrix
- Rows correspond to modes indexed by \( I \)
- Columns correspond to modes indexed by \( J \)
Separation Ranks of Convolutional Arithmetic Circuits

Recall expression for function realized by convolutional arithmetic circuit:

\[ h_y(x_1, \ldots, x_N) = \sum_{d_1 \ldots d_N=1}^{M} A_y^{d_1, \ldots, d_N} \prod_{i=1}^{N} f_{\theta_{d_i}}(x_i) \]

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- Rows correspond to modes indexed by \( I \)
- Columns correspond to modes indexed by \( J \)

Claim

\[ \text{sep}(h_y; I, J) = \text{rank}([A^y]_{I,J}) \]
Shallow Separation Ranks

Shallow convolutional arithmetic circuit (single hidden layer):

\[
\text{rep}(i,d) = f_{\theta_i}(x_i)
\]

\[
\text{conv}(j,\gamma) = \langle a^{0,j,\gamma}, \text{rep}(j,\cdot) \rangle
\]

\[
\text{pool}(\gamma) = \prod_{j \text{ covers space}} \text{conv}(j,\gamma)
\]

\[
\text{out}(y) = \langle a^{1,1,y}, \text{pool}(\cdot) \rangle
\]
Shallow Separation Ranks

Shallow convolutional arithmetic circuit (single hidden layer):

\[
\text{input } X \rightarrow \text{representation } M \rightarrow \text{hidden layer} \rightarrow \text{global pooling} \rightarrow \text{dense (output)}
\]

\[
\text{conv}(j, \gamma) = \langle a^{0,j,\gamma}, \text{rep}(j,:) \rangle \quad \text{pool}(\gamma) = \prod_j \text{conv}(j, \gamma) \quad \text{out}(y) = \langle a^{1,1,y}, \text{pool}(:,\gamma) \rangle
\]

Claim

\[
\text{rank}[\mathcal{A}^y]_{I,J} \leq r_0
\]

Proof sketch

Matricizing CP decomposition gives (\(\odot\) – Kronecker product):

\[
[\mathcal{A}^y]_{I,J} = \sum_{\gamma=1}^{r_0} a_{1,1,y}^{1,1} \cdot \left( \odot_{t=1}^{\|I\|} a_{0,i_t,\gamma}^{0,i_t,\gamma} \right) \left( \odot_{t=1}^{\|J\|} a_{0,j_t,\gamma}^{0,j_t,\gamma} \right)^\top
\]
Shallow Separation Ranks

Shallow convolutional arithmetic circuit (single hidden layer):

\[
\begin{align*}
rep(i,d) &= f_{\theta_i}(x_i) \\
\text{conv}(j,\gamma) &= \langle \mathbf{a}^{0,j,\gamma}, \text{rep}(j,: \rangle \\
pool(\gamma) &= \prod_{j \text{ covers space}} \text{conv}(j,\gamma) \\
\text{out}(y) &= \langle \mathbf{a}^{1,1,\gamma}, \text{pool}(:) \rangle
\end{align*}
\]

Claim

\[
\text{rank} \left[ A^\gamma \right]_{i,j} \leq r_0
\]

Shallow networks only realize separation ranks (correlations) linear in their size
Deep Separation Ranks

Deep convolutional arithmetic circuit \((L = \log_4 N\) hidden layers):

\[
\begin{align*}
&\text{input } X \\
&\text{representation} \\
&\text{hidden layer 0} \\
&\text{1x1 conv} \\
&\text{pooling} \\
&\vdots \\
&\text{hidden layer L-1} \\
&\text{(L=\log_4 N)} \\
&\text{1x1 conv} \\
&\text{pooling} \\
&\text{dense (output)} \\
&\text{output } Y
\end{align*}
\]

\[
\begin{align*}
rep(i, d) &= f_{\theta_i}(x_i) \\
\text{conv}_0(j, \gamma) &= \langle a^{0,j,\gamma}, \text{rep}(j,:) \rangle \\
\text{pool}_0(j, \gamma) &= \prod_{j' \in [4]} \text{conv}_0(j', \gamma) \\
\text{pool}_{L-1}(\gamma) &= \prod_{j' \in [4]} \text{conv}_{L-1}(j', \gamma) \\
\text{out}(y) &= \langle a^{L,1,\gamma}, \text{pool}_{L-1}(:) \rangle
\end{align*}
\]
Deep Separation Ranks

Deep convolutional arithmetic circuit ($L = \log_4 N$ hidden layers):

Theorem

Maximal rank that $[A^Y]_{I,J}$ can take is:

- **Exponential (in $N$) for “interleaved” partitions,**
  
  \[ e.g. \geq \min\{r_0, M\}^{N/4} \text{ for } I = \{1, 3, \ldots, N - 1\}, J = \{2, 4, \ldots, N\} \]

- **Polynomial (in network size) for “coarse” partitions,**
  
  \[ e.g. \leq r_{L-1} \text{ for } I = \{1, \ldots, N/2\}, J = \{N/2 + 1, \ldots, N\} \]
Deep Separation Ranks

Deep convolutional arithmetic circuit ($L = \log_4 N$ hidden layers):

```
input X  representation  hidden layer 0  ...  hidden layer L-1 (L=log_4 N)
           \          \           \             \          
rep(i,d) = f_{\theta_i}(x_i) \quad rep(j,\gamma) = \{a^{0,\gamma,rep(j,:)}\}
1x1 conv \quad pool_0(j,\gamma) = \prod_{j'\in\{j-I\}} conv_0(j',\gamma)
pool_{L-1}(\gamma) = \prod_{j'\in\{J\}} conv_{L-1}(j',\gamma)
out(\gamma) = \{a^{L,\gamma, pool_{L-1}(\gamma)}\}
```

**Theorem**

Maximal rank that $[A^\gamma]_{l,j}$ can take is:

- **Exponential (in $N$)** for “interleaved” partitions,
  
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- **Polynomial (in network size)** for “coarse” partitions,
  
  e.g. $\leq r_{L-1}$ for $I = \{1, \ldots, N/2\}$, $J = \{N/2 + 1, \ldots, N\}$

Deep networks realize exponential separation ranks (correlations) for favored partitions, polynomial (in network size) for others
Deep Separation Ranks Theorem – Proof Sketch

- For tensors $B, C$ with $P, Q$ modes resp, and a partition $T \cup S = [P + Q]$:

$$\left[ B \otimes C \right]_{T, S} = \left[ B \right]_{T \cap [P], S \cap [P]} \odot \left[ C \right]_{(T - P) \cap [Q], (S - P) \cap [Q]}$$

- Recursive application to the hierarchical decomposition of $A^\gamma$ gives:

$$\left[ \phi^{1, k, \gamma} \right]_{I_{1,k}, J_{1,k}} = \sum_{\alpha=1}^{r_0} a_{\alpha}^{1, \gamma} \cdot \bigotimes_{t=1}^{4} a_{0,4(k-1)+t, \alpha}^{0,4(k-1)+t, J_{0,4(k-1)+t}}$$

$$\ldots$$

$$\left[ \phi^{l, k, \gamma} \right]_{I_{l,k}, J_{l,k}} = \sum_{\alpha=1}^{r_l-1} a_{\alpha}^{l, \gamma} \cdot \bigotimes_{t=1}^{4} \left[ \phi^{l-1, 4(k-1)+t, \alpha} \right]_{l-1,4(k-1)+t, J_{l-1,4(k-1)+t}}$$

$$\ldots$$

$$\left[ A^\gamma \right]_{I,J} = \sum_{\alpha=1}^{r_L-1} a_{\alpha}^{L, \gamma} \cdot \bigotimes_{t=1}^{4} \left[ \phi^{L-1, t, \alpha} \right]_{L-1,t, J_{L-1,t}}$$

where $I \cup J = [N]$ is an arbitrary partition and:

$$I_{l,k} := (I - (k - 1) \cdot 4^l) \cap [4^l]$$

$$J_{l,k} := (J - (k - 1) \cdot 4^l) \cap [4^l]$$
Deep Separation Ranks Theorem – Proof Sketch (cont’)

\[
\begin{align*}
\left[\phi^1_{l,k,\gamma}\right]_{l_1,k,J_1,k} &= \sum_{\alpha=1}^{r_0} a_{\alpha}^{1,\gamma} \cdot \bigotimes_{t=1}^{4} \left[a_{0,4(k-1)+t,\alpha}\right]_{l_0,4(k-1)+t,J_0,4(k-1)+t} \\
&\vdots \\
\left[\phi^l_{l,k,\gamma}\right]_{l_l,k,J_l,k} &= \sum_{\alpha=1}^{r_l} a_{\alpha}^{l,\gamma} \cdot \bigotimes_{t=1}^{4} \left[\phi_{l-1,4(k-1)+t,\alpha}\right]_{l_{l-1},4(k-1)+t,J_{l-1},4(k-1)+t} \\
&\vdots \\
\left[A^y\right]_{l,j} &= \sum_{\alpha=1}^{r_L} a_{\alpha}^{L,y} \cdot \bigotimes_{t=1}^{4} \left[\phi_{L-1,t,\alpha}\right]_{l_{L-1},t,J_{L-1},t}
\end{align*}
\]

\[l_{l,k} := (l - (k - 1) \cdot 4^l) \cap [4^l], \quad J_{l,k} := (J - (k - 1) \cdot 4^l) \cap [4^l]\]

- Recall the rank-multiplicative property of the Kronecker product:
  \[\text{rank}(A \otimes B) = \text{rank}(A) \cdot \text{rank}(B)\]

- If partition \(I \cup J = [N]\) is “interleaved” then \(l_{l,k} \approx J_{l,k}\) and \(\left[\phi^l_{l,k,\gamma}\right]_{l_l,k,J_l,k}\) are approximately square, allowing ranks to grow double-exponentially fast.

- If partition \(I \cup J = [N]\) is “coarse” then either \(l_{l,k}\) or \(J_{l,k}\) is small, and the ranks of \(\left[\phi^l_{l,k,\gamma}\right]_{l_l,k,J_l,k}\) are limited.
The pooling geometry of a deep network links partitions \( I \cup J = [N] \) to spatial input patterns, thereby controlling the inductive bias:
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The **pooling geometry** of a deep network links partitions $I \cup J = [N]$ to spatial input patterns, thereby controlling the inductive bias:

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The **pooling geometry** of a deep network links partitions $I \cup J = [N]$ to spatial input patterns, thereby controlling the inductive bias:

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**Standard convolutional network design orients inductive bias towards statistics of natural images**
Conclusion

- Depth efficiency is complete with convolutional arithmetic circuits (SimNets), incomplete with convolutional rectifier networks.

- Shallow networks cannot model high correlation between input regions – require exponential size for exponential separation ranks.

- Deep networks can model with polynomial size exponential separation ranks for “favorable” partitions.

- Pooling geometry of a deep network determines which partitions are favorable, standard contiguous windows favor entangled partitions.
Thank You